Sains Malaysiana 40(3)(2011): 259–266

MEMS Very Low Capacitive Pressure Sensor Based on CMOS Process

(Sensor Kapasitif Bertekanan Sangat Rendah-MEMS Berasaskan Proses CMOS)

MUHAMAD RAMDZAN BUYONG*, NORAZREEN ABD AZIZ
& BURHANUDDIN YEOP MAJLIS

ABSTRACT

The CMOS standard process with advantage of simplicity in term of design and fabrication process compatibility has triggered the invention of MEMS very low capacitive pressure sensor, (MEMS-VLCPS). In this paper the development of the whole structure of MEMS-VLCPS that involves the design simulation, fabrication and testing is described. The novelty of this work lies in the design and fabrication process itself. A new technique in fabricating thin sensor membrane of VLCPS using seal-off techniques is also presented. The physical structure of the membrane consists of parallel plate. The top plate acts as the flexible electrode membrane and the bottom plate acts as the counter electrode membrane. Both plates are separated by absolute air gap with fixed end at both sides. As a result, it was found that the etch-opening holes of 0.8 µm and seal-off thickness of 4000 Å gave the optimum sealing surface. The percentage of relative capacitance change is extracted from the reference capacitance measurement. Air gap thickness of 0.3 µm gives the highest percentage of PRCC showing that smaller air gap thickness provides a larger change in capacitance value.

Keywords: CMOS; MEMS; very low capacitive pressure sensor

ABSTRAK

Proses piawai CMOS dengan kelebihannya dalam meringkaskan kesesuaian reka bentuk dan proses fabrikasi telah mencetuskan penciptaan sensor kapasitif bertekanan sangat rendah MEMS (MEMS-VLCPS). Di dalam kertas ini, pembangunan keseluruhan struktur MEMS-VLCPS yang melibatkan simulasi reka bentuk, fabrikasi dan uji kaji dibentangkan. Novelti penyelidikan ini terletak pada reka bentuk dan proses fabrikasinya yang tersendiri. Satu teknik baru dalam fabrikasi membran nipis sensor MEMS-VLCPS menggunakan teknik litupan juga diperkenalkan. Struktur fizikal membran terdiri daripada plat selari. Plat atas bertindak sebagai membran elektrod boleh lentur manakala plat bawah bertindak sebagai membran elektrod dengan pengimbang. Kedua-dua plat dipisahkan oleh rongga udara dengan kedua-duanya melekat pada sisi tepi. Melalui hasil pencirian, didapati bukaan rongga punar 0.8 µm dan ketebalan litupan sebanyak 4000 Å menghasilkan permukaan tertutup yang optimum. Peratusan perubahan kapasitan relatif, PRCC diperoleh melalui pengukuran kapasitan rujukan. Rongga udara berketebalan sebanyak 0.3 µm memberikan nilai PRCC paling tinggi yang menggambarkan rongga udara yang kecil menghasilkan perubahan yang besar dalam kapasitan.

Kata kunci: CMOS; MEMS; sensor tekanan kapasitif yang sangat rendah

INTRODUCTION

There is a trend to use surface micromachining as their advantage of CMOS process compatibility offers the possibility to reduce the size of total system.This can lower manufacturing cost, improve performance and provide the opportunities for application of MEMS structures in implantable biomedical devices. The development of a thin layer membrane in the area of capacitive pressure sensors is needed to measure small volume of intraocular pressure, (IOP) in human eye. IOP measurement is used for screening the risk of glaucoma that causes damage to the optic nerve which can gradually lead to vision loss (Snell & Lemp 1998). Measurements of the intraocular pressure are usually performed as single measurement at a certain time of the day. In order to have more frequent IOP measurement, an intraocular implant pressure sensor has been proposed to complement the current measurement technology (Mokwa 2003, 2007; Mokwa & Schnakenberg 2001). Due to the low IOP ranging from 10 mmHg to 75 mmHg, we proposed an appropriate miniaturized sensor i.e. very low capacitive pressure sensor (VLCPS) that would be beneficial to the user as it can produce accurate measurement.

The physical structure of VLCPS consists of a thin layer membrane, dielectric air gap and metal pad. Thin layer membrane was formed by two parallel plates with the top plate flexible while the bottom plate acts as a counter electrode. Both plates were separated by an absolute air gap which changers in the distances due to pressure applied that changes the capacitance value (Damghanian & Majlis 2009). Metal pad was used to connect the bottom and top plate for measuring the capacitance between two electrodes under pressure applied. The novelty of this work lies in the thin layer membrane formation as it uses surface micromachining technology that promises compatibility in CMOS standard process. The fabricated sensor is proposed to be mounted in a wearable contact lens as shown in Figure 1. In this paper the development of the whole structure of MEMS-VLCPS that involves the design simulation, fabrication and testing are discussed.

SIMULATION

The deflection mechanism of the membrane under applied pressure rangging from 10 mmHg to 1000 mmHg was analyzed using CoventerWare simulator. Figure 2 (a and b) show the 3D simulation structure of thin membrane, while Figure 2 (c) shows the manhattan bricks meshing structure used in the simulation.

As evaluation, the deflection of the thin layer membrane was analyzed using mathematical modelling based on a simple square solid plate (Ganji & Majlis 2004). Two parameters were introduced in the equation to compensate the additional features on the sealed-off proses. The first is t, a coefficient used to compensate the added stiffness on the structure due to seal-off silicon nitride film. The latter is ξ, a coefficient for decrease in stiffness resulted from cutting etch holes on the thin layer membrane plate (Hamzah et. al 2004). Simulated and calculated values of deflection increase proportionally to the pressure applied as shown in Figure 3. This shows that simulation and mathematical modeling has similar correlation under the pressure applied.

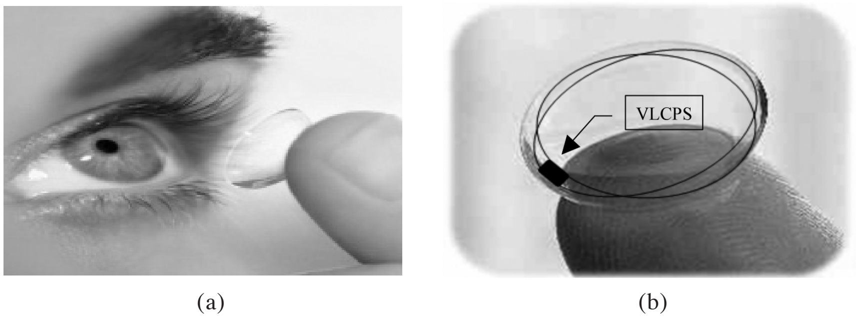


FIGURE 1. (a and b). The fabricated sensor is mounted in the contact lens in order to measure pressure in the eye for glaucoma analysis

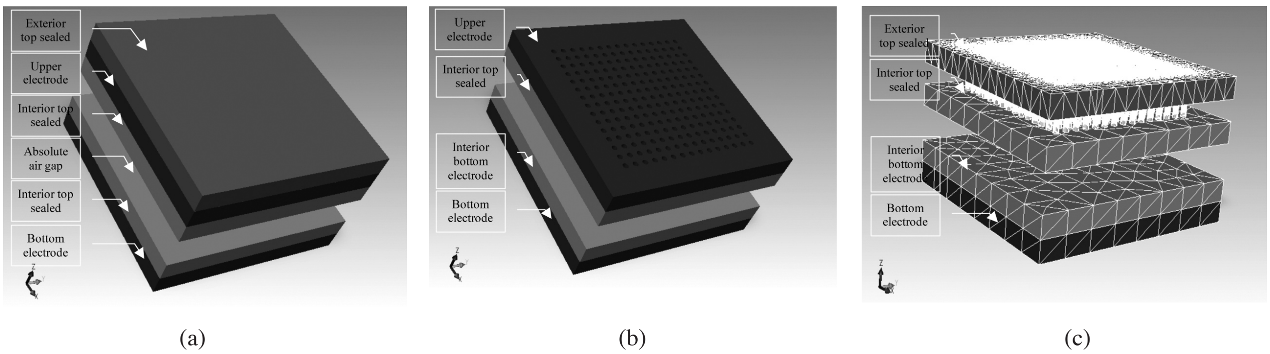


FIGURE 2. Simulation structure of (a) 3D simulation using Coventorware, (b) hide exterior top seals layer and (c) hide upper electrode and meshed

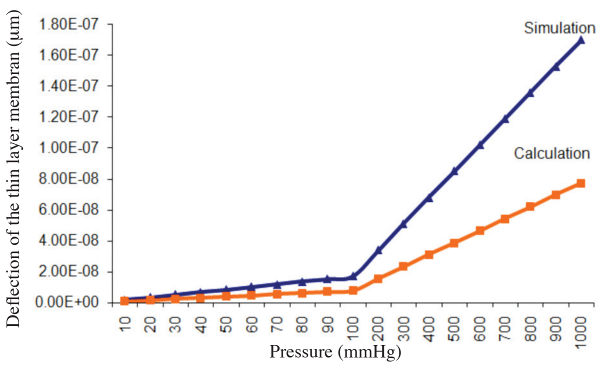


FIGURE 3. Simulated and calculated deflection of the thin layer membrane versus applied pressure

FABRICATION PROCESS

Based on CMOS standard process, the first step for the fabrication of MEMS-VLCPS is to form the thin membrane as shown in Figure 4(a). This step involves three stages; (1) opening the multi holes etch of top plate, (2) removing the sacrificial intermediate oxide underneath the top plate for dielectric air gap development and (3) closing the etch holes using deposition method (Buyong et al. 2008). The holes should be big enough for the etchants to pass through to remove the sacrificial oxide layer. However, it must be able to be closed later to form flexible membrane. The second step is to form the contact opening on the top and bottom plate as shown in Figure 4(b). The final step is to form metal pad on both plate for the connection as shown in Figure 4(c).

The first stage of the fabrication process starts with the insulator formation of oxide layer followed by depositing silicon nitride film using low plasma chemical vapor deposition (LPCVD) method. A doped polysilicon layer was then deposited on top of the silicon nitride film which was then patterned and etched to form the bottom electrode. Next, another nitride layer was deposited on top of the first doped polysilicon plate followed by the deposition of sacrificial doped oxide, which was deposited using plasma enhanced chemical vapor deposition (PECVD). Another silicon nitride layer was deposited on top of the sacrificial oxide layer followed by deposition of doped polysilicon layer which acts as top electrode plate. These two layers were patterned into circular array shape and etched using reactive ion etching (RIE) method. Dielectric air gap can be obtained by removing the enclosed sacrificial oxide layer using buffered oxide etch (BOE) via the multi holes opening etch windows. The opening holes were then sealed with silicon nitride using LPCVD.

The second stage of the fabrication process is continued with the development of metal contact as it is needed in providing the connection path between sensor structures and external connection. The process starts with the formation of contact opening for bottom electrode followed by the formation of contact opening for the top electrode. Both process uses RIE technique with different etching time since the bottom contact electrode is deeper compared to the top contact electrode. The schematic diagram for both contact holes is shown in Figure 4(b).

The final stage of the device fabrication is metallization process which requires several deposition steps. Titanium and titanium nitride was deposited to improve the adhesion between polysilicon electrodes with the next metal layer. Then, rapid thermal annealing (RTA) took place for silicide formation. Subsequently, aluminum silicon copper (AlSiCu) and TiN was deposited on top of the Ti and TiN layer. AlSiCu layer acts as intermediate material between electrode and the external connection. TiN layer acts as Anti Reflective Coating (ARC) for the next lithography process as aluminums is a highly reflective material. Metal pad for both bottom and top contact electrode was patterned by lithography process and etched using RIE metal etcher. The schematic diagram of the whole structure is shown in Figure 4(c).

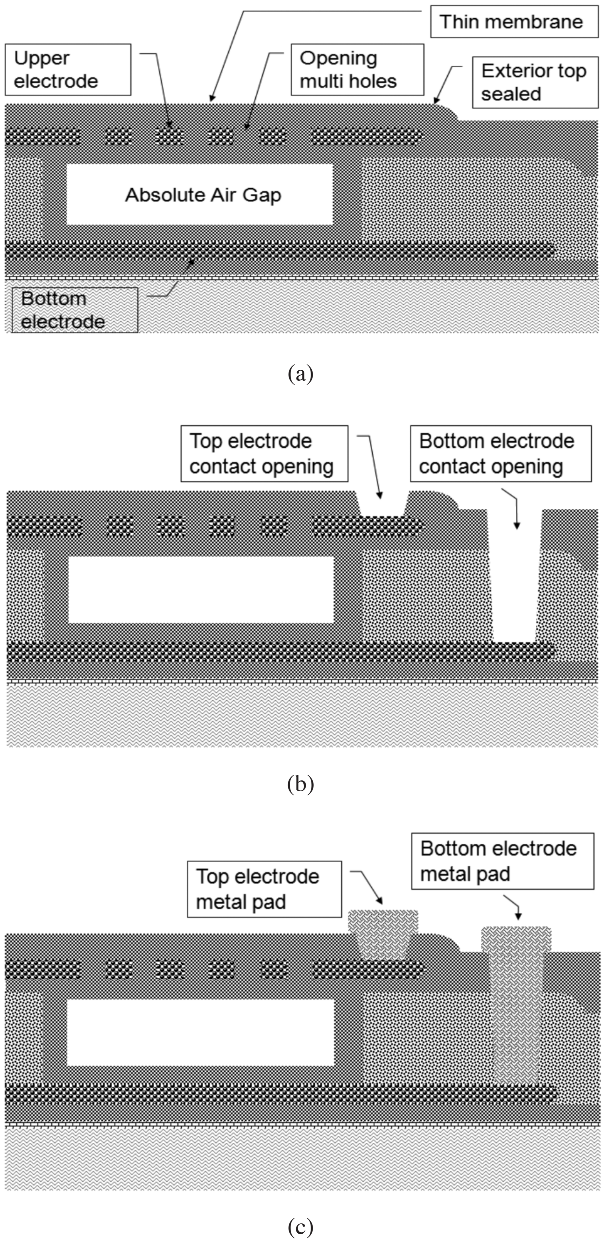


FIGURE 4. Formation of (a) thin layer membrane, (b) contact holes and (c) metal pad

Each stage uses the CMOS standard process flow and facilities. Figure 5 shows the fabrication process flow chart while Figure 6 shows the actual images of overall structure of VLCPS. The fabricated thin membrane comprises dielectric air gap structure as shown in Figure 7. Figure 8 shows the metal pad that was used as a connector for capacitance measurement.

The challenge in this work was the technique to fabricate thin membrane which acts as part of the capacitive pressure. The method used in fabricating the thin membrane structure is surface micromachining method

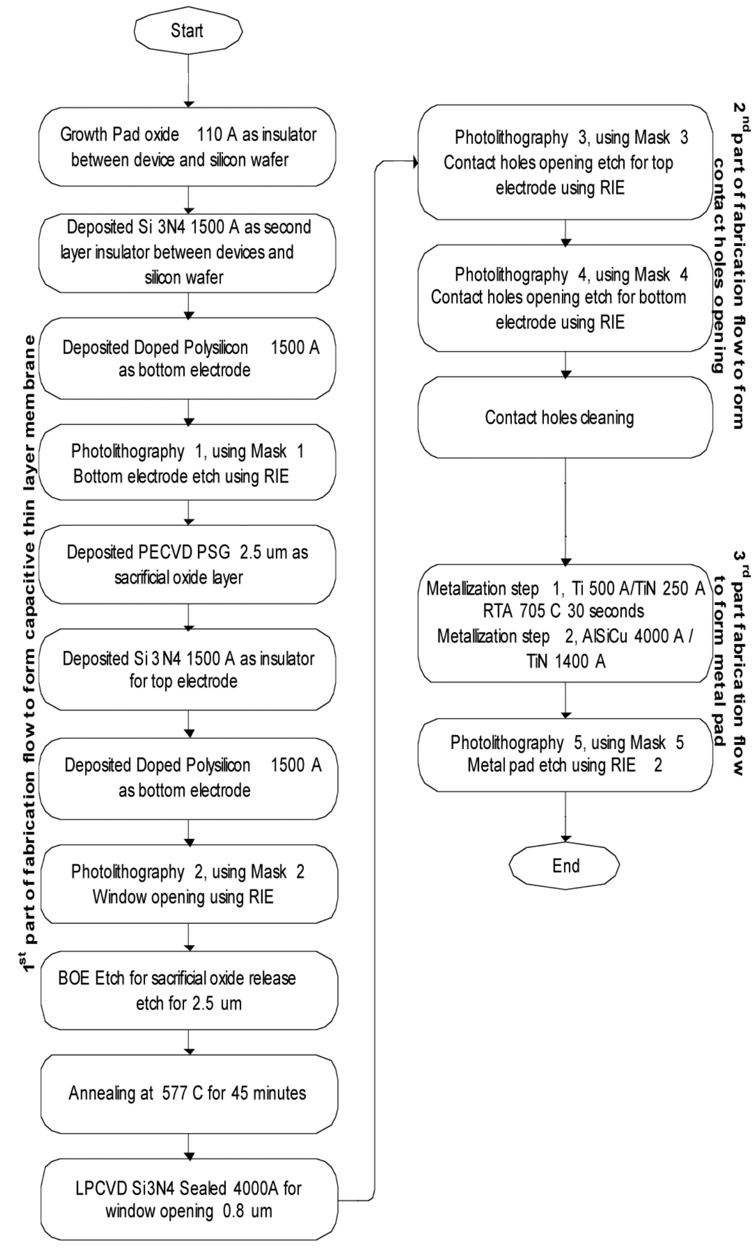


FIGURE 5. Fabrication proses flow chart

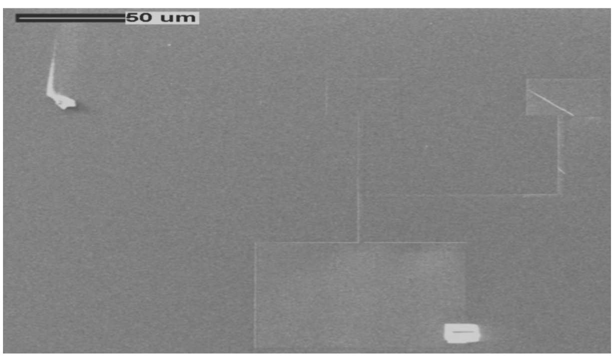


FIGURE 6. Overall structure of VLCPS

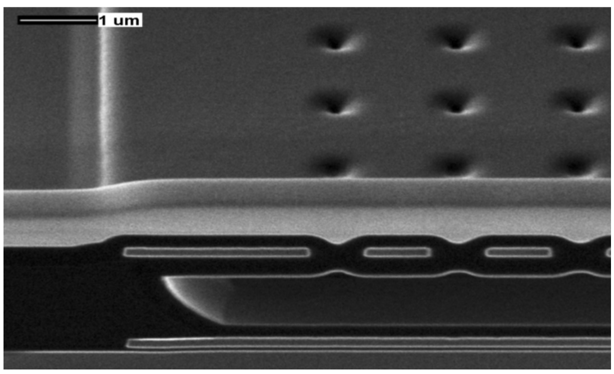


FIGURE 7. Thin membrane

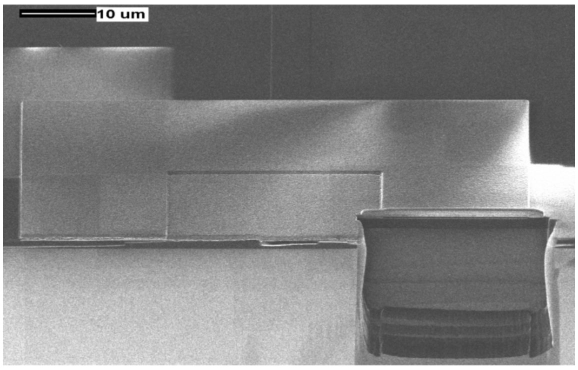


FIGURE 8. Metal pad

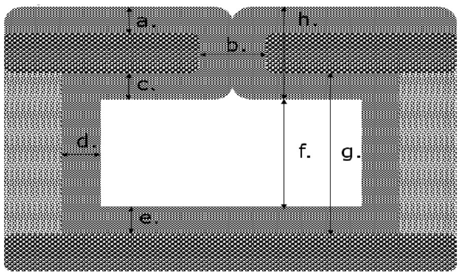


FIGURE 10. Illustration of sealed-off process

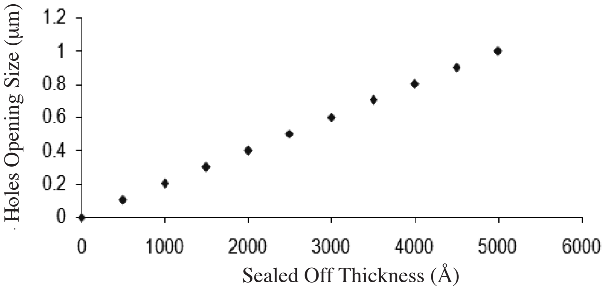


FIGURE 11. The co-relation graph between holes opening with sealed thickness

using polysilicon as the structural layer. A sealed cavity (absolute air gap) was sandwiched between two electrodes. The structure was embedded by sacrificial oxide layer which was removed later. The optimized thin membrane was achieved by (1) characterization of anisotropic etching process for opening etch access window, (2) isotropic sacrificial oxide removal and (3) characterization of sealing process of the opening etches windows using LPCVD technique. Figure 9 shows the process to fabricate the thin membrane utilizing multi etch access windows as follow: (a) wafer preparation with multiple film stack, (b) dry etching of polysilicon and silicon nitride films for opening etch windows, (c) isotropic sacrificial oxide removal by wet etching and (d) sealing off etch windows by nitride deposition.

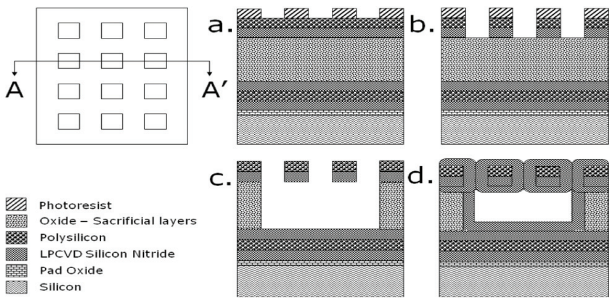


FIGURE 9. Proposed process flow of the thin layer membrane

The hypothesis assumes that an optimum thickness for sealing process would be achieved when the thickness of interior (top: c, sidewall: d and bottom inner sealed: e) and exterior (top membrane sealed: a) is identical, as shown in Figure 10. Since LPCVD silicon nitride is based on the diffusion process, it means that the deposition of the thin film should be conformal on the exposed surface area (Maier et al. 1995; Maier et al. 1996). If the deposition thickness of interior and exterior is less than half of the etch-opening holes sizes, then the sealing process will not be complete.

Figure 11 shows the plot of sealing process versus etch opening holes size. It shows that higher seal-off silicon nitride thickness is needed for bigger etch-opening holes size. It was found that the etch-opening holes of 0.8 µm and seal-off thickness of 4000 Å gave the optimum sealing surface. Based on the plotted data we can conclude that the ratio of holes etch-opening holes to the sealed thickness is 2:1 (Buyong et al. 2009).

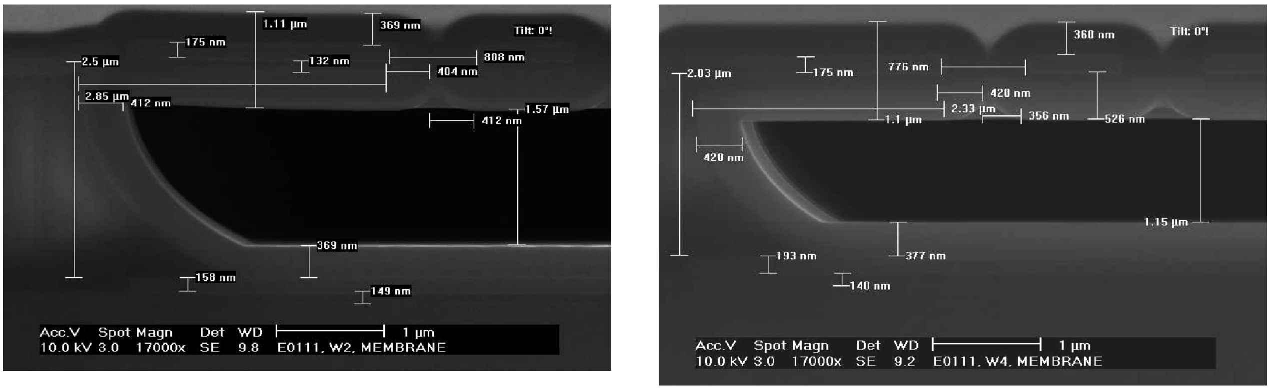
Figures 12 and 13 show the scanning electron microscope (SEM) images of the thin membrane layer for various air gap thicknesses. It is proven that the optimum etch-opening holes of 0.8 µm and seal-off thickness of 4000 Å provides a complete sealing surface for various membrane air gap thicknesses.

The cross sectional focus ion beam (FIB) image of complete structure of VLCPS in Figure 14 shows the fabricated membrane having 1 µm of layer thickness. Overall fabrication process step is well matched with CMOS processes.

DEVICE TESTING

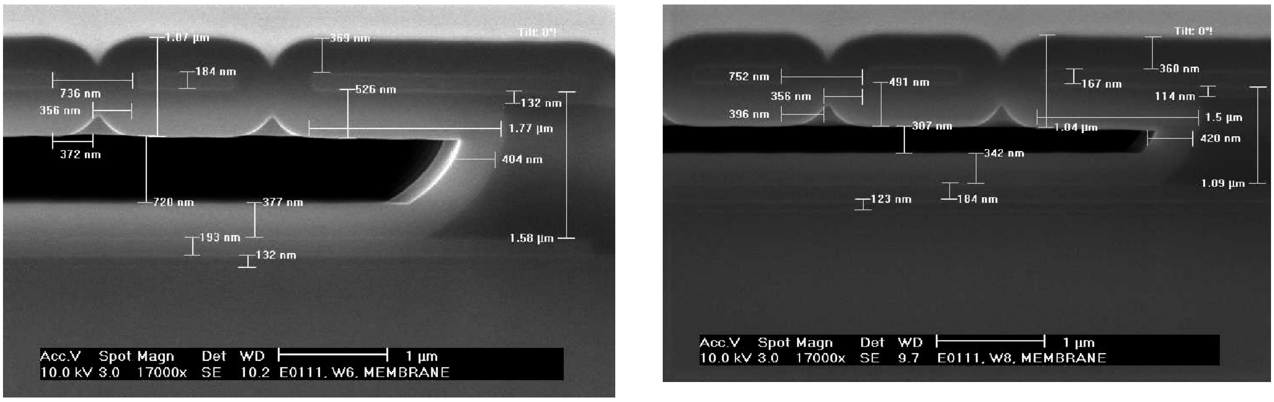
A capacitance measurement is used to test the functionality of the fabricated device. For this purpose, the metal pad of VLCPS structure is connected to Agilent E4980A Precision LCR Meter to measure the reference capacitance. Two probes connected to the metal pad are used for measuring the reference capacitance as shown in Figure 15. Voltage biases were swept from 2 Vrms to -2 Vrms at frequency of 1 MHz.

Changes in the deflection of the membrane affects the distance of the top electrode and bottom electrode, thus also affects the capacitance value. Figure 16 shows the plot of reference capacitance under two circumstances;



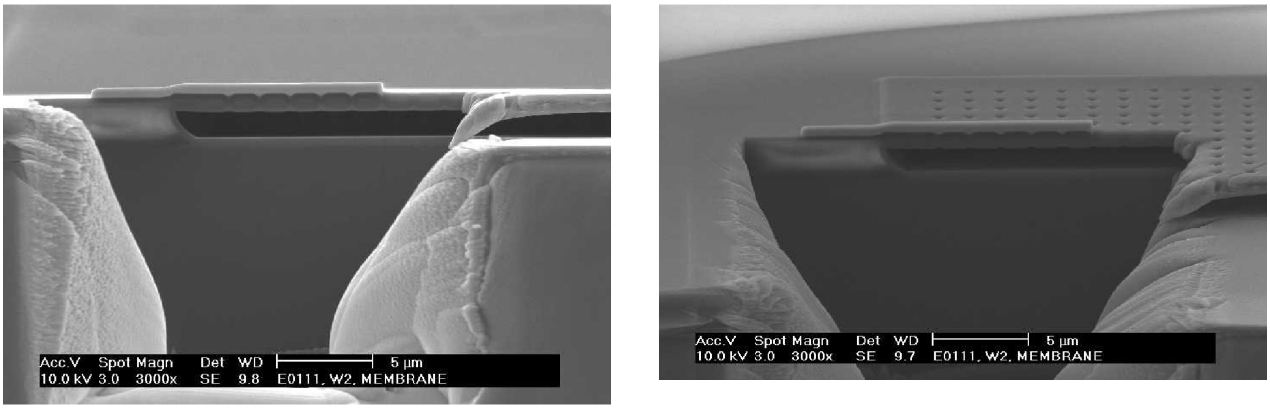
(a) (b)

FIGURE 12. SEM image of thin layer membrane, 0.8 μm hole opening and sealed with 4000 Å silicon nitride for air gap size of (a) 1.5 μm and (b) 1.15 μm



(a) (b)

FIGURE 13. SEM image of thin layer membrane, 0.8 μm hole opening and sealed with 4000 Å silicon nitride for air gap size of (a) 0.7 μm and (b) 0.3 μm



(a) (b)

FIGURE 14. (a and b) FIB images of CMOS-based MEMS parallel plate capacitive sensor

calculation and measurement. Reference capacitance is calculated using equation (1) without deflection for various air gap thicknesses:

$$C_{reference\ measurement} = \varepsilon_r \varepsilon_o \frac{A}{d_{reference}}. \quad (1)$$

where ε_r, relative permittivity of dielectric material between the plates, εo, permittivity of free space 8.854 × 10^{-12} F/m, A, cross sectional area of plate and d, distance between top and bottom electrode. Figure 17 shows $d_{reference} - d_{deflection}$.

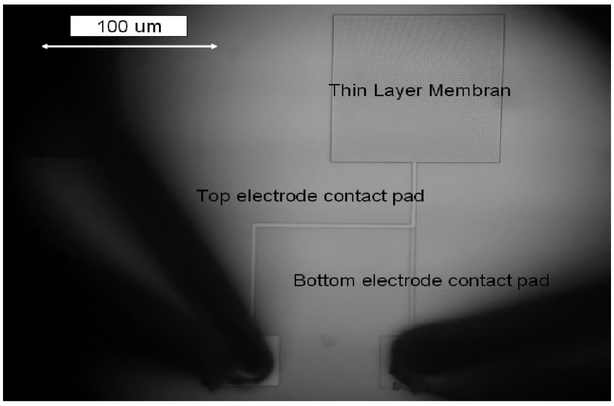


FIGURE 15. Reference capacitance measurement on VLCPS contact pad

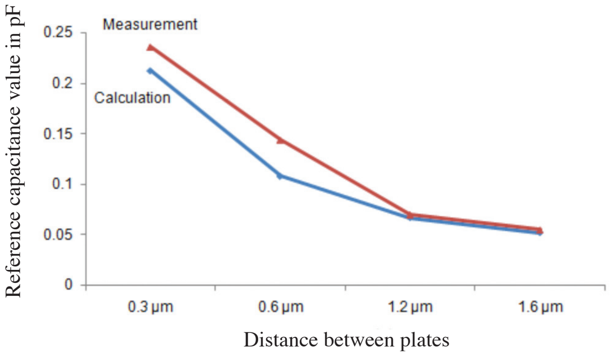
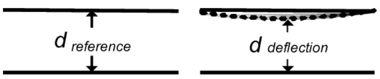


FIGURE 16. Comparison of the reference capacitance value by calculation and measurement



$$d_{new} = d_{reference} - d_{deflection}$$

FIGURE 17. Definition for $d_{new} = d_{reference} - d_{deflection}$

The reference capacitance of the completed structure was measured without applying any pressure on both electrodes. It is shown in the graph that there is not much significant difference between the measured and calculated reference capacitance.

The difference between capacitance value under pressure applied and the references capacitance value results to a percentage relative change in capacitance (PRCC) as given in equation (2).:

$$PRCC = \frac{C_{new,\,measurement} - C_{reference,\,measurement}}{C_{reference,\,measurement}} * 100, \qquad (2)$$

when

$$C_{new,\,calculation} = \varepsilon_r \varepsilon_o \frac{A}{d_{new}}.$$

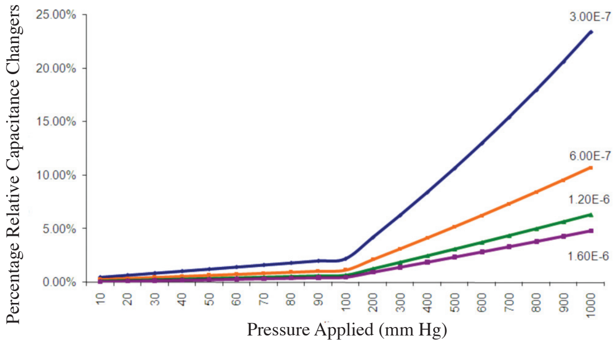


FIGURE 18. PRCC behavior versus pressure applied with various air gap thicknesses

The percentage of relative change of the capacitance value for various air gap thicknesses is plotted in Figure 17 under pressure applied ranging from 10 mmHg to 1000 mmHg. Air gap thickness of 0.3 µm gave the highest PRCC followed by 0.7 µm and 1.2 µm while air gap thickness of 1.6 µm gives the lowest PRCC. It can be concluded that as we increase the thickness of the VLCPS air gap, the PRCC will be decreased.

CONCLUSION

A complete structure of very low capacitive pressure sensor, VLCPS has been successfully fabricated using CMOS standard process. The process development of the sensor-membrane using surface micromachining has been characterized and optimized. It was found that the etch-opening holes of 0.8 µm and seal-off thickness of 4000 Å gave the optimum sealing surface. Air gap thickness of 0.3 µm gives the highest percentage of PRCC showing that smaller air gap thickness provides bigger change in capacitance value.

REFERENCES

Buyong, M.R., Aziz, N.A. & Majlis, B.Y. 2008. Fabrication of thin layer membrane using CMOS process for very low pressure sensor application. *Proc. IEEE International Conferences on Semiconductor Electronics*, pp. 320-326.

Buyong, M.R., Aziz, N.A. & Majlis, B.Y. 2009. Characterization and optimization of seals-off for very low pressure sensor VLPS fabricated by CMOS MEMS process. *Advanced Materials Research* 74: 231-234.

Damghanian, M. & Majlis, B.Y. 2009. Novel design and fabrication of high sensitivity MEMS capacitive sensor array for finger print imaging. *Advanced Materials Research* 74: 239-242.

Ganji, B.A. & Majlis, B.Y. 2004. Modeling of diaphragm for micromachined condenser microphones. *Proc. 2004 IEEE International Conferences on Semiconductor Electronics*, pp. 15-21.

Hamzah, A.A., Majlis, B.Y. & Ahmad, I. 2004. Deflection analysis of epitaxially deposited polysilicon encapsulation for MEMS devices. *Proc. IEEE International Conferences on Semiconductor Electronics*, pp. 611-614.

Maier, D., Koprululu, A., Holm, B.S. & Obermeier, E. 1996. Elastic properties and microstructure of LPCVP polysilicon films. *Journal of Microelectromechanical and Microengineering* 6: 436-44.

Maier, D., Maibach, J., Obermeier, E. & Schneider, D. 1995. Variations in Young's modulus and intrinsic stress of LPCVD polysilicon due to high-temperature annealing. *Journal of Microelectromechanical and Microengineering* 5: 121-124.

Mokwa, W. 2003. Ophthalmic implants. *Proc. IEEE Sensors* 980-986.

Mokwa, W. 2007. Medical implants based on microsystems. *Measurements Science Technology* 18(5): R47-R57.

Mokwa, W. & Schnakenberg, U. 2001. Micro Transponder systems for medical applications. *IEEE Transactions on Instrumentation and Measurement* 50(6): 1551-1555.

Snell, R.S. & Lemp, M.A. 1998. *Clinical Anatomy of the Eye*. Boston: Blackwell Science.

Institute of Microengineering and Nanoelectronics (IMEN)
Universiti Kebangsaan Malaysia,
43600 UKM Bangi, Selangor D.E.
Malaysia

*Corresponding author; email: muhdramdzan@yahoo.com

Received: 16 July 2010
Accepted: 3 September 2010